REMARKS

Claims 1, 6 and 7 have been amended. Claim 12 has been cancelled without prejudice or disclaimer. Claims 1, 3-7 and 9-11 are pending and under consideration. Claims 1, 6 and 7 are the independent claims. No new matter is presented in this Amendment.

CLAIM OBJECTIONS:

Claims 1, 6 and 7 are objected to because of minor informalities.

Applicants have amended claims 1, 6 and 7 to correct the minor informalities noted by the Examiner. Claim 7, for example, has been amended to delete the term "offset regions having no doping" in order to be consistent with the change of claim 1 made in the amendment filed on May 14, 2010. Applicants have also amended claims 1 and 6 to correct the minor antecedent basis issues noted by the Examiner.

REJECTIONS UNDER 35 U.S.C. §102:

Claims 6, 7 and 9-12 are rejected under 35 U.S.C. §102(b) as being anticipated by Oka et al. (U.S. Patent No. 6,184,541).

Regarding the rejection of independent claim 6, it is noted that claim 6, as amended, recites

> A thin film transistor (TFT) comprising:
> a channel region;
> source and drain regions respectively formed at opposite sides of the channel region;
> lightly doped drain (LDD) or offset regions formed at respective opposite sides of the channel region and between the source and drain regions ;and
> a plurality of primary crystal grain boundaries,
> wherein the thin film transistor is formed so that the primary crystal grain boundaries of a polysilicon substrate are positioned in the channel, source and drain regions but not positioned in the LDD or offset regions, and
> wherein a **width of** the **LDD** or offset regions **is less than** a **distance between two adjoining primary crystal grain boundaries**.

The Office Action relies on Oka and in particular in FIGS. 1(a) and 1(b) for a teaching of a channel region (8), source and drain regions (5), and a lightly doped drain (LDD) region or

offset region (portion of region 4 having a width d in FIG. 1(b)).

The Office Action further states that the primary crystal grain boundaries (2) are positioned in the channel (8), source and drain regions (5) but not positioned in the LDD or offset regions (d) and that a width (*d*) of the LDD or offset regions is less than a distance between two adjoining primary crystal grain boundaries (2).

Accordingly, the Office Action relies on the effective length "*d*" of the low concentration region 4, illustrated in FIG. 1(b) of Oka, for a teaching of an LDD region or an offset region, and relies on the high concentration regions (5) for a teaching of source and drain regions.

However, Applicants note that Oka teaches that when the grain size is longer than the length "D" of the low concentration region, the high concentration impurity diffuses deeply along the grain boundary, thereby shortening an effective length "d" of the low concentration region. As a result, an OFF effect of the TFT switching characteristics is lowered. Even the TFT is in an OFF state, when the LCD is subjected to a high temperature, a leakage current enough to produce micro brighter spots runs between the source and the drain of TFT (*see* Col. 2, Ln 15-24 of Oka).

Accordingly, Oka teaches away from forming the width of the LDD or offset regions to be less than a distance between two adjoining primary crystal grain boundaries, since such formation would produce a leakage current.

Therefore, as a solution the above mentioned problem, Oka teaches setting a length "D" of the low concentration region not shorter than an average grain size of the polycrystal silicon film (*see* Col. 3, Ln 51-54). Oka further states that an effective length "d" of the low concentration region is thus restrained from being shorter, therefore, an OFF-current that is a TFT switching characteristic is decreased, and a leak current between source and drain is restrained (*see* Col 3, Ln 66–Col. 4, Ln 3). In essence, Oka maintains the length of the low concentration region to be "D," and thus the offset or LDD region is "D" and not "d" as noted by the Examiner.

Accordingly, the primary crystal grain boundaries of the polysilicon substrate are positioned in the LDD or offset regions, contrary to the recitation of independent claim 6. Therefore, since Oka clearly teaches that the LDD or offset region is "D" Applicants respectfully note that there is no basis in the reference to specify that the effective length is "d," as suggested by the Examiner.

Accordingly, Applicants respectfully assert that Oka fails to teach or suggest, at least, this novel feature of independent claim 6.

As noted in MPEP 2131, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). In the instant case, the LDD regions or offset regions being disposed and directly contacting the channel region and the source and drain regions respectively are neither expressly nor inherently taught by Oka.

Regarding the rejection of independent claim 7, it is noted that claim 7, as amended, recites

> A flat panel display device comprising:
> a thin film transistor comprising:
> a channel region;
> offset regions formed at opposite sides of the channel region;
> source and drain regions respectively formed at outer sides of the offset regions; and
> a plurality of primary crystal grain boundaries,
> wherein the thin film transistor is formed so that the primary crystal grain boundaries of a polysilicon substrate are not positioned in the offset regions, and
> wherein a width of the offset regions, is smaller than a distance between the primary crystal grain boundaries.

As noted above, the Office Action relies on the effective length "*d*" of the low concentration region 4, illustrated in FIG. 1(b) of Oka, for a teaching of an offset region, and relies on the high concentration regions (5) for a teaching of source and drain regions.

As also noted above, Oka does not teach or suggest that the width of the offset regions is smaller than a distance between the primary crystal grain boundaries, and furthermore that the primary crystal grain boundaries of the polysilicon substrate are not positioned in the offset regions.

Accordingly, Applicants respectfully assert that Oka fails to teach or suggest, at least, this novel feature of independent claim 7.

Regarding the rejection of claims 9-11, it is noted that these claims depend from independent claim 7, and as noted above, Oka fails to teach or suggest the novel features of independent claim 7.

Accordingly, Applicants respectfully assert that the rejection of dependent claims 9-11 under 35 U.S.C. §102(b) should be withdrawn, at least, because of their dependency from claim 7, and the reasons set forth above, and because the dependent claims include additional features which are not taught or suggested by the prior art. Therefore, it is respectfully submitted that claims 9-11 also distinguish over the prior art.

Regarding the rejection of independent claim 12, it is noted that claim 12 has been cancelled without prejudice or disclaimer. Accordingly, the rejection of claim 12 is moot.

REJECTIONS UNDER 35 U.S.C. §103:

Claims 1 and 3 are rejected under 35 U.S.C. §103(a) as being unpatentable over Oka et al. (U.S. Patent No. 6,184,541).

Regarding the rejection of independent claim 1, it is noted that claim 1 recites:

> A thin film transistor (TFT) comprising:
> a channel region having a plurality of primary crystal grain boundaries;
> source and drain regions formed at respective ends of the channel region; and
> offset regions one of which is formed between the channel region and the source region and the other one of which is formed between the channel region and the drain region,
> wherein the thin film transistor is formed so that the primary crystal grain boundaries of a polysilicon substrate are not positioned in the offset regions, and
> wherein a width of each one of the offset regions is smaller than a distance between the primary crystal grain boundaries formed in the channel region.

Regarding the rejection of independent claim 1 it is noted that this claim recites some substantially similar features as claims 6 and 7. Thus, the rejection of this claim is also traversed for similar reasons as set forth above.

Accordingly, Applicants respectfully assert that Oka fails to teach or suggest, at least, this novel feature of independent claim 1.

Regarding the rejection of claim 3, it is noted that this claim depends from independent claim 1, and as noted above, Oka fails to teach or suggest the novel features of independent claim 1.

Accordingly, Applicants respectfully assert that the rejection of dependent claim 1 under 35 U.S.C. §103(a) should be withdrawn, at least, because of its dependency from claim , and

the reasons set forth above, and because the dependent claim includes additional features which are not taught or suggested by the prior art. Therefore, it is respectfully submitted that claim 3 also distinguishes over the prior art.

CONCLUSION:

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 503333.

Respectfully submitted,

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Date: October 22, 2010

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